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(1)

In reply refer to SC77-352

October 20, 1977

To: Air Force Office of Scientific Research
Bolling Air Force Base
Washington, DC 20332

Attention: NE

SUBJECT: Quarterly Technical Report No. 1 for period May 1, 1977 thru August 31, 1977

In accordance with the requirements stated for Contract No. F49620-77-C-0087, enclosed herewith is the First Quarterly Technical Report.

ROCKWELL INTERNATIONAL CORPORATION
SCIENCE CENTER

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ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

Quarterly Technical Report No. 1
for period 05/01/77 through 08/31/77

Contract No. F49620-77-C-0087

General Order No. 5110

Project No. 3384

Rockwell International/Science Center
Thousand Oaks, California 91360

Sponsored by

Advanced Research Projects Agency (DOD)
ARPA Order No. 3384
Monitored by AFOSR Under Contract # F49620-77-C-0087

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Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (W

REPORT DOCUMENT

D INSTRUCTIONS COMPLETING FORM

1. REPORT NUMBER

AD-A186 764

CATALOG NUMBER

4. TITLE (and Subtitle)

ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

5. TYPE OF REPORT & PERIOD COVERED
Quarterly Technical Report
05/01/77 through 08/31/77

6. PERFORMING ORG. REPORT NUMBER
SC5110.2QR

7. AUTHOR(s)
R. Zucca, F. Eisen, R. Eden, B. Welch, J. Kruger, R. Fairman, and D. Ch'en

8. CONTRACT OR GRANT NUMBER(s)
F49620-77-C-0087

9. PERFORMING ORGANIZATION NAME AND ADDRESS
ROCKWELL INTERNATIONAL CORP./SCIENCE CENTER
1049 Camino Dos Rios
Thousand Oaks, CA 91360

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
ARPA Order No. 3384

11. CONTROLLING OFFICE NAME AND ADDRESS
Advanced Research Projects Agency (DOD)
1400 Wilson Boulevard
Arlington, VA 22209

12. REPORT DATE
October 20, 1977

13. NUMBER OF PAGES
64

14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)
Air Force Office of Scientific Research
Bolling Air Force Base
Washington, DC 20332

15. SECURITY CLASS. (of this report)
Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES
This research was sponsored by the Advanced Research Projects Agency (DOD)
ARPA Order No. 3384

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Semi-Insulating GaAs
Ion Implantation
IC
Integrated Circuits

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the first quarter results of a program designed to develop a planar process technology for GaAs integrated circuits. Planar structures will be achieved by ion implantation into localized areas of semi-insulating substrates to form device areas with proper electrical characteristics. Caltech, Cornell University, and Crystal Specialties, Inc. are subcontractors in this program.

In bulk crystal growth, progress in eliminating causes of boat wetting has led to a more stable substrate fabrication process with 65% yield.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20. Evaluation of alternative sources of substrate material have been initiated. A wafer preparation process that yields the flatness required by projection lithography (better than 2μm) has been developed.

In ion implantation we have concentrated on work related to achieving high doping levels in FET source and drain regions. Se implantation has been studied in order to determine the optimum dose for these highly doped regions, consistent with a single (850°C) anneal for both the channel and contact implants. The study of Si implantation as an alternate method of doping contacts has been initiated.

Planar 1μm gate FETs and planar level shifting diodes have been fabricated. The devices have good dc characteristics. This demonstrates that the fabrication of isolated devices into implanted pockets embedded into semi-insulating GaAs substrates is a workable approach.

A mask set with numerous fabrication tests, evaluation of component design alternatives, and simple circuits (linear chains and ring oscillators) has been designed and was being fabricated at the end of the reporting period. A computer controlled system for dc measurements on fabrication test features and circuit components is under construction. Preliminary results on FET modeling for the study of switching parameters are presented.

FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell Science Center as the prime contractor with two universities and a crystal growth company as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. Program manager is F. Blum. The principal investigators for each organization are:

Science Center	D. R. Ch'en
California Institute of Technology	J. W. Mayer, M-A. Nicolet
Cornell University	L. F. Eastman
Crystal Specialties	W. P. Allred

Numerous other researchers are involved in the work reported on. The principal contributors are:

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California Institute of Technology	J. Tanden
Cornell University	M. Shur
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1.0 INTRODUCTION

A number of military and other government needs require digital integrated circuits cabable of operation at higher speeds with lower power consumption than is possible with the present silicon technologies. Applications include digital communication, navigation, radar signal processing, etc. Silicon devices are rapidly approaching their fundamental limitations in power and speed. In order to meet future needs of high performance integrated circuits the use of new materials is required. The high electron mobility of GaAs combined with the availability of semi-insulating substrate material make it an attractive choice on which to base a new integrated circuit technology. In order to realize the full potential of GaAs integrated circuits for high speed, low power applications, it is essential to develop the capability of producing such circuits with LSI complexity.

The present program is designed to develop an ion implanted planar IC process technology, reaching MSI complexibility at the end ot the first phase of 17 months duration. It is anticipated that this process technology would be extended to LSI capability during a second phase of approximately 18 months. The use of a planar process involving ion implantation is strongly indicated by the need to develop a process capable of yielding circuits of

LSI complexity. Ion implantation is required for GaAs ICs because of the difficulties associated with diffusion of impurities into GaAs. In addition, the reproducibility and uniformity of ion implantation doping of GaAs, which has been demonstrated in our past work, will be essential in producing LSI circuits.

The present program requires efforts in a number of different areas including the growth of semi-insulating GaAs substrates to increase yield and boule size, the optimization of ion implantation techniques, the development of processing and process monitoring techniques, and the development of test features and their automatic testing. ICs will be fabricated in order to evaluate the results of the process development efforts. Although the bulk of this research effort is carried out at the Science Center, some valuable cooperation is received by three subcontractors. These are Crystal Specialties Inc. in GaAs substrate growth, the California Institute of Technology in some aspects of ion implantation, and Cornell University in device modeling.

During the first quarter of the program, progress has been made in the growth of semi-insulating GaAs qualified as an ion implantation substrate. Experiments have been initiated on the effects of gettering treatments on semi-insulating GaAs. Our use of a projection mask aligner to carry out the photolithography steps required for IC fabrication imposes

severe requirements on the flatness of the substrate material used in our process. We have developed the ability to prepare wafers of sufficient flatness and to maintain this flatness during the various steps of the fabrication process.

The fundamental soundness of our proposed fabrication process has been demonstrated during this quarter by the successful fabrication of planar FETs and Schottky diode structures. Implantation work has been carried out to determine optimum implant conditions for achieving high doping levels in high contact regions, and an investigation of the applicability of silicon implantation to GaAs ICs has been initiated.

In order to evaluate processing techniques which we developed, it is necessary to fabricate various test structures and simple circuits. We have designed a mask set to be used in fabricating such test vehicles and released the design to the mask fabricator. This mask set contains test patterns to monitor the fabrication process, a variety of device designs in order to develop design rules, and some simple circuits for preliminary speed measurements.

A large number of measurements on test circuits which are fabricated to evaluate our process development are required. In order to accomplish this in an efficient manner, work was initiated on an automatic dc test system. It is anticipated that this system will be operational during the

second quarter of the work on this contract. Work has been initiated at Cornell University on the theoretical analysis of the switching speed of GaAs ICs. The results of this work will be incorporated into the design effort for test circuits as the development effort proceeds.

2.0 TECHNICAL SUMMARY

The goal of this program is to develop an ion implanted planar technology for GaAs integrated circuits. The need for such a technology becomes apparent when one realizes that silicon technology is reaching the speed limit dictated by fundamental material properties. GaAs, with its more favorable velocity-electric field characteristic and a semi-insulating substrate is the most attractive replacement for Si. This has been demonstrated by the development of a discrete GaAs microwave device technology. This technology has matured to the point that integration has become technically feasible.

This program is based on the success of a previous DARPA program under which a reproducible technology for ion implantation into semi-insulated GaAs substrates has been developed. The circuits will be fabricated by ion implantating directly into localized areas of the semi-insulating substrate to form device areas with proper electrical characteristics. By performing multiple implantation steps, we will tailor the electrical characteristics of each device area to the device requirement. Therefore, we expect to achieve a planar structure and an optimum device design at the same time and without compromise. This program requires a blend of continued research effort on substrate fabrication and

implantation technology with the development of processing techniques and process monitoring tests, the development of design rules, and the design, fabrication and evaluation of test circuits. This work is carried on by the Science Center with the support of three subcontractors.

The following is a summary of the accomplishments of each program task in the first quarter. Details will be found in the following sections of the report.

1. Bulk Crystal Growth. (Sec. 3.1) This activity carried on at Crystal Specialties has resulted in a more stable substrate fabrication process. Yield fluctuations, have decreased as the causes of boat wetting are gradually being understood. Yield of good quality single crystal semi-insulating GaAs is 65% of which 94% resulted electrically compensated. Material has been delivered to the Science Center on a regular basis.

2. Evaluation of Alternative Sources of Semi-Insulating GaAs. (Sec. 3.2) In this task, carried out at the Science Center, the principal yardstick was the ability of the material to pass the qualification tests for ion implantation. In addition to the Crystal Specialties material of which 71% was qualified, material from Morgan Semiconductor (two boules)

passed the qualification tests satisfactorily, while Sumitomó material (only one boule tested) failed to pass the test.

3. Gettering Treatment of Semi-Insulating GaAs. (Sec. 3.3) Gettering, both by ion bombardment and by impact sound stressing has been pursued at the Science Center as an attempt to improve semi-insulating substrates which were not qualified for ion implantation. The first experiments have been unsuccessful.

4. Wafer Flatness. (Sec. 3.4) In order to achieve the flatness required by the projection mask aligner used for photolithography (better than 2μm), substrate preparation techniques have been developed at the Science Center. The required flatness has been achieved by determining an optimum wafer thickness (0.025 inches), and by developing a process for etching and dielectric coating the front and back of the wafer achieving good stress relief.

5. Ion Implantation. (Sec. 4.1) This work, carried on at the Science Center, was aimed at finding an optimum dose for high doping level implants such that they can be annealed simultaneously with the low dose implants used for FET

channels. An optimum dose range near $5x10^{13}$ ions/cm^2 has been found, and it will be more precisely resolved in the future. In cooperation with Caltech, study of Si implantation has been initiated. Si appears as a good candidate to replace Se for fabrication of high carrier concentration regions, with anneal temperature more compatible with the low dose implants than heavy dose Si implants, for room temperature implants.

6. Device and Circuit Fabrication. (Sec. 4.2) Planar 1μm gate FETs and planar level shifting diodes have been fabricated at the Science Center by the proposed process of implantation into localized areas of the material. The devices had good dc characteristics. Although these devices were fabricated using a single implant, no major difficulty is expected in extending the proces to multiple implants.

7. Mask Design. (Sec. 4.4) A mask set has been designed at the Science Center, and it was being fabricated at the end of the reporting period. This mask set is designed for a three implant process, with the option of using only two of them. The layout contains numerous fabrication tests, evaluation of component design alternatives, and simple circuits (linear chains and ring oscillators) for preliminary speed measurements.

8. Automatic Test System. (Sec. 5.1) Such a system, based on an Electroglas 1034X automatic prober controlled by a minicomputer, is under construction at the Science Center. It will be used for a large volume of dc measurements on fabrication test features and circuit components.

9. Switching Speed Analysis. (Sec. 5.2) At Cornell University a two-dimensional computer model for the electron dynamics in the channel of a GaAs FET has been developed. This model will be used to study the switching parameters for GaAs FETs.

3.0 MATERIALS

The requirements for semi-insulating GaAs substrates were developed during an earlier program RADC-TR-77-136, "Investigation of Technological Problems in GaAs," where specific attention was devoted to the evaluation of semi-insulating GaAs for the purpose of ion implantation. Through this study, a stringent qualification test was developed that has in all cases shown a distinct difference between usable ingots and those whose semi-insulating properties are marginal.

The specification for semi-insulating GaAs wafers for integrated circuit fabrication is based upon the following:

I. Physical Properties

A. High quality single crystal, chromium compensated GaAs, free from crystalline imperfections, inclusions, and precipitates.

B. Large cross-sectional area (1.5 in^2).

C. (100) oriented wafers cut to $\pm 1/2^{o}$.

D. Etch pit density $<10^4$ cm^{-2},

E. Surface preparation:

1. Flat, damage-free polish on one side with back side of wafer lapped and etched for damage and stress relief
2. Wafer flatness of $\pm 2\mu m$ across each wafer and parallelism of $\pm 25\mu m$ across each wafer

II. Electrical Properties

A. Bulk Resistivity - A resistivity $\rho > 10^7$ ohm cm is required from the as grown crystals.

B. Thermal Anneal - A sheet minimum resistance of $10^7 \Omega/\square$ is required from samples cut from the front and rear of each ingot following an anneal at 850 C for 30 minutes, in which the wafer was capped with 1200 Å of reactively sputtered Si_3N_4.

C. Implantation Damage Anneal - A minimum sheet resistance of $10^6 \Omega/\square$ is required from samples cut from the front and rear of each ingot following bombardment with $3 \times 10^{12} cm^{-2}$, 300 KeV Krypton ions at 200 C and annealed as described in II.B.

3.1 Bulk Crystal Growth of Semi-Insulating GaAs (Crystal Specialties)

Growth of high quality single crystals by the Horizontal Bridgmann Technique depends on tight control of several variables. Among these, the most crucial is boat wetting. Boat wetting not only affects the crystallinity of the crystal, it also affects the etch pit count, compensation and thermal conversion.

Boat wetting is usually caused by an OH^- ion which acts as a bond between the quartz and the GaAs. Purposeful additions of H_2O, H_2, and hydrocarbons all grossly enhance boat wetting. Hydrogen, which combines with residual O_2, produces the OH^- radical. Likewise, hydrocarbons are reduced at high temperatures, producing hydrogen and OH^- ions.

The major source of OH^- is found in the quartz tubing used to manufacture the quartz boats and ampoules. Analysis of the quartz reveals about 5 ppm of OH^- absorbed in the quartz lattice. Attempts to remove the OH^- by vacuum heat treating has not proved successful.

A method currently used to reduce boat wetting is to let the molten GaAs stay in contact with the quartz boat for as long as 96 hours. Why this long soak time is beneficial is not understood. It has also been suggested that a quartz phase called crystabalite, which grows on the surface of the boat during the soak period, reduces the wetting.

The degree of wetting has a direct correlation upon the dislocation density observed in the crystal. Wetting causes strain in the plastic crystal lattice. This is caused by the different expansion of the quartz boat and the GaAs crystal. The difference in expansion causes slip within the lattice. If wetting is severe, it results in a polycrystalline growth. Less severe wetting causes a rise in the dislocation density. At the present time good crystals have an etch pit count of between 1000 and 10,000cm^{-2}.

High resistivity (10^7-10^8 ohm-cm) GaAs is obtained by doping the crystal with chromium. The ability to compensate melt grown GaAs is determined by the residual free carrier concentration of the undoped GaAs. The most prominent impurity observed is silicon. Silicon comes from dissociation of the quartz boat and ampoule. The level of silicon in horizontal Bridgmann growth is about $1x10^{15}$ carrier/cm^3. If the silicon content approaches the chromium concentration, the material will not be compensated.

It has been observed that when wetting is severe, our ability to compensate is affected. This may be related to the fact that the SiO resulting from the dissociation of SiO_2 is volatile and transports into the GaAs melt.

Thermal conversion appears to be tied to the wetting problem. It has been observed that when wetting is excessive, the number of crystals

which convert upon heat treating also increases. This is also due to the contamination of the GaAs melt.

During the past report period, our single crystal yield was 65%. That is 65% of the chromium doped crystals grown met the specifications. This yield is felt to be quite acceptable although there have been periods where single crystal yield was considerably higher. The percentage of compensated material was very high during this same period. The number of compensated ingots was 94%.

Eighty percent, of the crystals that were heat treated for thermal conversion by customers, did not convert.

A heat treating system to test for conversion will be added to the Crystal Specialties facilities. It is planned that wafers from all chromium doped cyrstals will be tested for conversion before being sent to the Science Center.

3.2 Evaluation of Alternative Sources of Semi-Insulating GaAs (Science Center

During this first quarter, two additional GaAs sources were evaluated from GaAs wafers delivered to the specification outlined in Section 3.0. Morgan Semiconductor, Inc., and Sumitomo Electric Industries, Ltd., were sampled by evaluation of wafers cut from the front and tail of

each ingot. The availability of material from both alternate sources was good. The physical properties were within our specification except for wafer flatness which was 6 μm on the Sumitomo and 10 μm on the Morgan material.

The electrical qualification of all the ingots tested during this period is shown in Table 3.2-1. The yield of fully qualified semi-insulating ingots from Crystal Specialties was 71% during this period. Both Morgan Semiconductor ingots passed the qualification tests successfully. However, a larger number of ingots need to be tested before any yield figures are determined.

Sumitomo Electric material did not qualify for the electrical specifications. It will be sampled again during the next period.

Chromium doped GaAs has been requested from Laser Diode, Inc., but no material has been available during this reporting period.

In summary, semi-insulating GaAs substrates have been received and accepted that meet the physical and electrical specifications for integrated circuit development. Electrical qualification was shown by Crystal Specialties, Inc., and Morgan Semiconductor, Inc. Wafer flatness was marginal from all subcontractors, however, 2.1 x 2.1 cm samples could be cut from wafers supplied by Crystal Specialties that were within the 3μm flatness specification. Improvements in the flatness and electrical yield of qualified substrates will be pursued during the next period.

Table 3.2-1

Substrate Qualification for Ion Implantation

Sheet Resistance (Ω/□)

VENDOR	Front No Kr	Front Kr	Tail No Kr	Tail Kr	
Crystal Specialties Inc.					
#3463	10^8	10^8	10^8	10^8	
3475	10^8	10^8	10^8	10^8	
3473	10^8	10^8	10^8	10_8	
3436	$1x10^5$	$8x10^3$	10^8	10^8	*Rejected
3474	10^8	10^8	10^8	10^8	
3396	10^8	10^8	10^8	10^8	
3405	10^3	$1.3x10^3$	10^8	10^5	*Rejected
Sumitomo Electric Ltd.					
FS20370	$2x10^3$	$1x10^5$	$2.5x10^4$	$5x10^4$	*Rejected
Morgan Semiconductor Inc.					
MS 5-26	10^8	10^8	10^8	10^8	
MS 2-31	10^8	10^8	10^8	10^8	

3.3 Gettering Treatment of Semi-Insulating GaAs (Science Center)

Gettering treatments involving the introduction of damage on one side of a wafer, followed by suitable annealing, have been used by severalworkers to remove impurities or defects from Si and improved its properties. For example, copper has been shown to collect at damage sites introduced by ion bombardment of Si.[1] Schwuttke[2] has shown that significant improvements in the lifetime of Si can be achieved using a damage treatment called impact sound stressing, followed by the annealing which takes place in normal processing of Si devices. Recently it has been shown that ion bombardment gettering treatment of semi-insulating GaAs can affect the doping level in epitaxial layers grown on the gettered material,[3] and can reduce compensation of n-type implanted layers observed using some semi-insulating substrates.[4] We have attempted to determine whether or not gettering treatment of semi-insulating GaAs which does not pass the qualification tests can be improved by gettering treatments. Both ion bombardment and impact sound stressing have been used in this work.

Bombardment with 400 keV Krypton ions to doses of 10^{14} or 10^{15} ions/cm^2 at room temperature has been used to introduce damage for gettering experiments. Substrate material was taken primarily from Crystal Specialties boule #2299, which did not pass the above mentioned qualification tests. The bombarded side of the wafer was coated with 1000Å of reactively

sputtered silicon nitride covered with approximately 2000Å of sputtered silicon dioxide. The first experiments involved annealing at 850°C for a period of 16 hours. Following the anneal, AuGe contact dots were applied and alloyed. Initial measurements indicated a low resistance between the contacts. Etching experiments in which GaAs was removed while the contacts were protected from etching indicated that the conducting region produced by the bombardment and anneal treatment penetrates to a depth of at least 250 micrometers. Subsequent experiments were carried out using reduced annealing temperatures or reduced times at 850°C. The wafers used usually had polished backsides which were capped with silicon nitride during annealing. Annealing at 850°C for 60 min. or at 750°C for 16 hours has been found to produce a surface conductivity which can be removed by etching of no more than 5 micrometers from the bombarded surface. We have performed a qualification test on material treated in this way by capping the treated surface with silicon nitride and annealing at 850°C for 30 min. Formation of a conducting surface layer has been observed in all experiments carried out to date.

Experiments have also been carried out using materials which was impact sound stressed by Dr. G.H. Schwuttke at IBM. The treated side of the material was coated with silicon nitride and the other polished surface was cleaned and etched in the manner usually used before a qualification test.

That surface was then coated with reactively sputtered Si_3N_4 and samples were annealed at 850°C for several different times and at 900°C for 30 min. The 850°C anneals included one for 30 minutes which is the time normally used in qualification tests. In these experiments, also, a conducting layer was formed on the surface of the GaAs for all anneal sequences employed.

In the experiments carried out so far, we have not observed any indication that it is possible to produce qualified GaAs substrates from initially unqualified material. We expect to pursue this further by using samples from other unqualified boules and by varying the bombardment and anneal cycles.

3.4 Substrate Flatness (Science Center)

GaAs substrate flatness criteria is established by the depth of focus as determined by the Canon 4:1 Projection Mask Aligner used for the photolithography (Sec. 4.2). To resolve a 0.8 μm line in a 0.5 μm positive photoresist layer an overall flatness of 3 μm is required.

In order to accomplish this degree of flatness, every aspect of processing must be considered in relation to substrate deformation. The wafer flatness has been checked at the following fabrication stages:

(1) As received.

(2) After cleaning and polishing.

(3) After Si_3N_4 deposition (1200Å).

(4) After annealing at 850°C, 30 minutes.

In the initial stage of the program, a Sloan Diamond stylus, "Dektak" was used to measure wafer flatness in two directions. The resolution offered by this instrument was $\pm$ 50Å. The Dektak was used to make preliminary measurements in order to screen out the major problems and was later replaced with a non-destructive optical interference measurement. The optical interference approach utilized an optical flat and a 5461Å Hg light source. A Polaroid camera was set up to provide a 2:1 photographic base to record the results of each subsequent processing step.

The measurements revealed the following:

(1) As-received wafers were typically 10-20 μm "concave".

(2) Chemical etching produced 10-15 μm convex shapes.

(3) Si_3N_4 deposition (1200 Å) induced further convex deformation.

(4) Subsequent annealing of (3) produced extreme convex deformation

Each of the above problem areas was studied individually and were resolved in the following manner:

(1) Initial wafer flatness: Improvement in polishing procedures by Crystal Specialties and other vendors brought the surface

flatness to a 4-10μm level, from where smaller samples (2.1 x 2.1 cm as required for processing) could be cut with the specified flatness better than 3 μm.

(2) All chemical etching in GaAs is anisotropic due to the differential etch rates for the high index planes. In order to create a less preferential etch rate, a chem-mechanical process employing bromine-methanol was selected for polish damage removal. The resultant surface finish was featureless and near identical to the initial flatness, except for some edge rounding, as shown in Figure 3.4-1. The surface damage was evaluated with a preferrential etch to delineate any subsurface work damage. Inspection of an in-process test chip revealed no noticeable damage by optical interference contrast microscopy.

(3) The stress induced by Si_3N_4 (1200Å) in all cases produce compressive forces which result in a convex deformation of the treated surface. In order to counteract the Si_3N_4 stress a backside coating was applied to balance the forces prior to any high-temperature annealing. Total wafer deformation is also related to wafer thickness. Samples of the following thicknesses were tested: 0.017 in., 0.020 in., 0.025 in., and 0.030 in. No differences were observed between the 0.025 in.

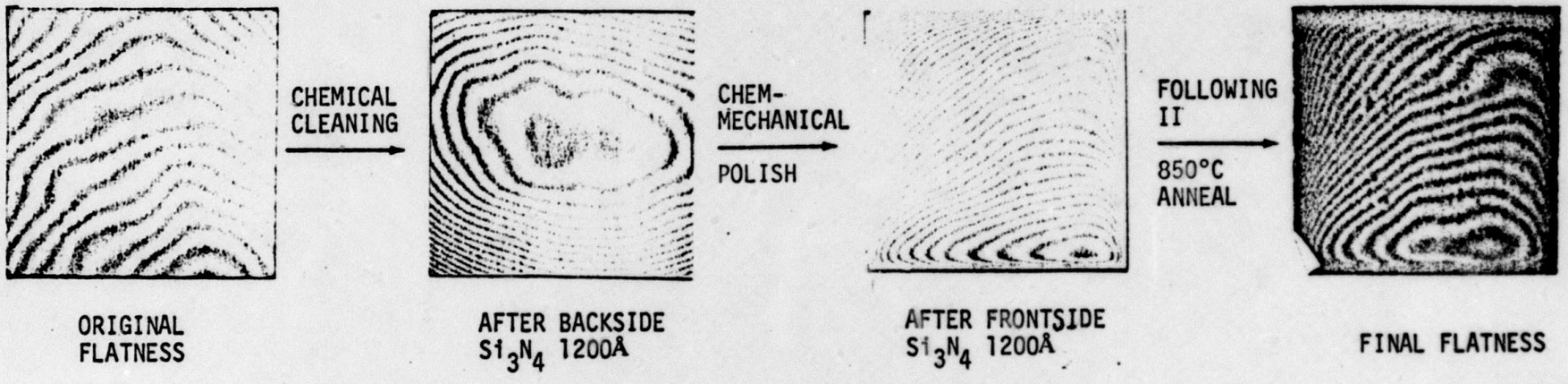

Fig. 3.4-1 GaAs wafer flatness thru several processing steps

and 0.030 in. wafers. Whereas, the 0.017 in. and 0.020 in. samples were more easily deformed. All subsequent work has, therefore, been done with 0.025 in. thick wafers. Initially the polished wafers were supplied with an "as-cut" backside. Annealing these wafers at 850°Cshowed some deformation due to the strain and crystal damage effects. Experiments with wafers that were lapped and chemically etched on the backside showed very little deformation through the high-temperature anneal.

The major conclusions concerning flat (100) GaAs processing can be summarized as follows:

(a) Selection of initial flat sample with damage-free finish, flat to $3\mu m$.

(b) Wafer thickness must be 0.025 in. and the wafers must be free of backside damage.

(c) Si_3N_4 coatings must be first applied to the back side of the wafer following a chemical cleaning.

(d) Flat, chem-mechanical polish with 0.05% Br_2-methanol solution is required.

(e) Frontside Si_3N_4 layer should be applied immediately after the top side polishing and cleaning.

The control of surface flatness throughout the present process is shown in Figure 3.4-1. The process is reproducible. The final flatness is limited only by the initial wafer flatness.

4.0 PROCESS DEVELOPMENT

This section will cover the fabrication stages, starting from ion implantation in Section 4.1 and continuing with device and circuit fabrication in Section 4.2. In Section 4.3 a contact metalization study will be presented. Finally, in Section 4.4, a mask set recently designed will be described.

4.1 Ion Implantation

As discussed in Section 4.4, the new masks designed for IC process development give us the option of carrying out a heavy dose n-type implant (called n^{++}) in selected areas of the IC chip such as source and drain regions of the FETs. The processing of ICs making use of such an implant would be simplified if the implant could be carried out at room temperature and if the annealing could be performed at the same temperature as the annealing for the two other more lightly doped implants (called n and n+). With these objectives in mind, the activation of Se implants in the dose range between 10^{13} and 10^{14} ions/cm^2 has been explored in some detail, and and investigation of the doping profiles resulting from Si implantation in GaAs has been initiated. The details of this work are given in the two following subsections.

4.1.1 Selenium Implantation (Science Center)

Low dose Se and S implants are used for the n- and n+ implants respectively for ICs fabricated with our new IC mask set (See Sec. 4.4). Satisfactory activation of these implants can be obtained by annealing at 850°C for 30 min. As mentioned above, we also have the capability in the new mask design to make use of n++ implants in contact regions. It is desirable to be able to accomplish the annealing of all three implanted regions in a single anneal step. Past work with low dose implants indicates that the doping profile is not greatly changed when the annealed temperature is increased to 900°C. A 900°C anneal is expected to result in greater activation of n++ implants; again, based upon the results of past work on Se implantation.[5] It, however, is desirable to accomplish the annealing of the implanted wafers at as low a temperature as possible. One factor is connected with the adherence of the silicon nitride layer which must remain upon the GaAs wafer during the entire fabrication process. While we have successfully annealed GaAs at temperatures as high as 950°C using a silicon nitride cap, we believe that there will be fewer problems with the adherence of the silicon nitride layer if annealing is carried out at temperatures below 900°C. Annealing at 850°C is not expected to yield the highest possible activation of a high dose Se implant. However, such activation is not necessary to accomplish the purpose of the n++ implant on the IC chips.

A doping level of a few x10^{17}cm^{-3} with a sheet resistance lower than that of the FET active region by a factor of 3 or 4 should be sufficient. With this in mind, the activation of Se implants as a function of dose has been examined for anneals carried out at 850°C, and 875°C. Previous work has indicated that the activation of high dose Se implants may actually decrease as the dose is increased beyond a certain point. We therefore, wish to identify the dose resulting in minimum sheet resistance and/or maximum activation of the implanted dopant. Minimization of the implanted dose may also be important in maintaining the integrity of the silicon nitride layer through which the Se is implanted since a lower dose means lower damage to the silicon nitride.

The sheet resistance, sheet electron concentration and effective mobility measured for samples implanted with 300 KeV Se ions at 200°C are shown in Fig. 4.1-1. Annealing was carried out at 850°C or 875°C. The mobility is seen to decrease somewhat as the Se dose is increased. The sheet electron concentration shows a maximum at 4 to 5x10^{13} ions/cm^2. The result is that there is a broad minimum in the sheet resistance of the implanted layer at a dose near 4x10^{13} ions/cm^2. A dose as low as 3x10^{13} ions/cm^2 appears to be adequate to produce a satisfactory sheet resistance for the n++ implants. Annealing at 875°C produces a small decrease in sheet resistance, but the advantage gained is probably not

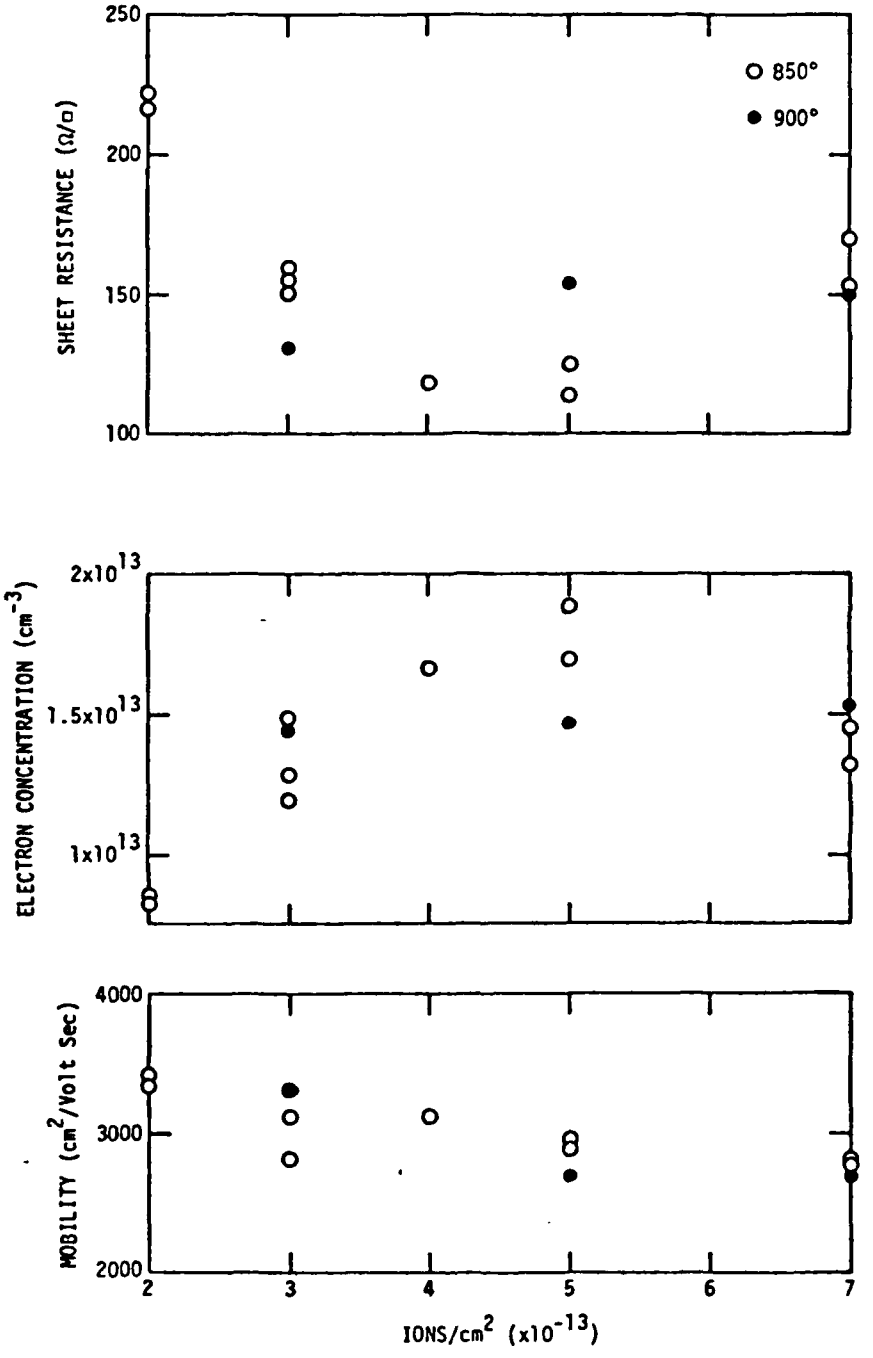

Fig. 4.1-1 Sheet resistance, electron concentration, and electron mobility as a function of the dose of 300 KeV Se ions implanted at 200°C and annealed at the indicated temperatures

sufficient to warrant increasing the anneal temperature for implanted IC wafers. It is desirable to have electron concentration and mobility profile data for samples implanted with doses near $3x10^{13}$ ions/cm^2 Such Figure measurements will be carried out in the near future. However, the results of past experiments with higher dose implants suggest that the electron concentration profile is probably fairly flat, maintaining a constant value almost to the surface of the implanted wafer.[5] If this is found to be the case, implanted doses of about $3x10^{13}$ ions/cm^2 will satisfy the requirements of the n^{++} IC implants. The present work has been carried out at an implant temperature of 200°C. It is desirable to be able to carry out the implants at room temperature. The implant temperature dependence of Se implants with doses near $3x10^{13}$ions/cm^2 will be investigated in the near future.

4.1.2 Silicon Implantation (Caltech and Science Center)

Our past work has indicated that it is necessary to carry out high dose implants of group VI dopants at elevated temperatures (approx. 200°C or higher) in order to obtain good activation of the implanted dopant. The processing of GaAs IC circuits would be simplified if the n^{++} implants could be carried out at room temperature. It has been reported that the activation of high dose Si implants is higher when they are carried at room

temperature than when they are performed at elevated temperatures.[6] However, there is very little information available as to the activation of Si implants in GaAs as a function of the dose of implanted Si and as to the doping profiles resulting from Si implantation in GaAs. Therefore, an investigation of Si implantation in GaAs has been undertaken. The implants have been performed on the 400 KeV accelerator at Caltech. Capping and annealing were carried out at the Science Center and profiling measurements using anodization and stripping with sequential Hall coefficient and resistivity measurements have been carried out at Caltech.

The first implants were performed at room temperature with a Si beam energy of 400 KeV. Implantation doses were 10^{13}, 10^{14}, and 10^{15} ions/cm^2. Annealing was carried out with both reactively sputtered silicon nitride and sputtered silicon dioxide caps at temperatures at 850°C and 900°C. Measurements of the approximate sheet resistance as a function of dose, annealing cap, and annealing temperature are given in Table 4.1-1. The data indicates that slightly lower sheet resistances can be obtained using the silicon nitride cap as compared to the silicon dioxide cap, and that low sheet resistances can be obtained utilizing an 850°C, 30 min. anneal. Electron concentration and mobility profile data are contained in Figs. 4.1-2 and 4.1-3 for some of the samples listed in Table 4.1-1. Maximum electron concentrations of 10^{18}/cm^{-3} or greater were obtained in three of the four

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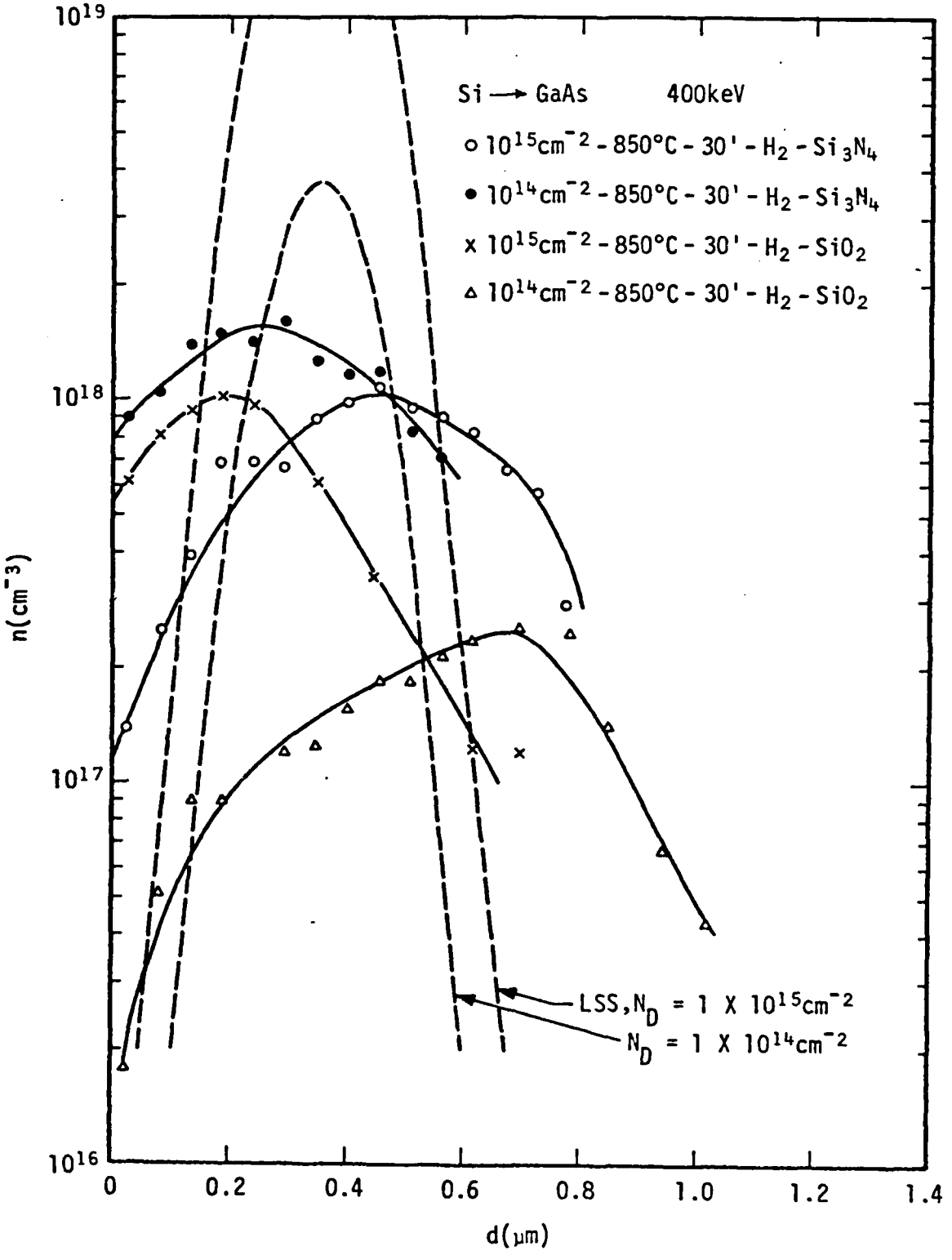

Fig. 4.1-2 Carrier concentration profiles in Si implanted GaAs

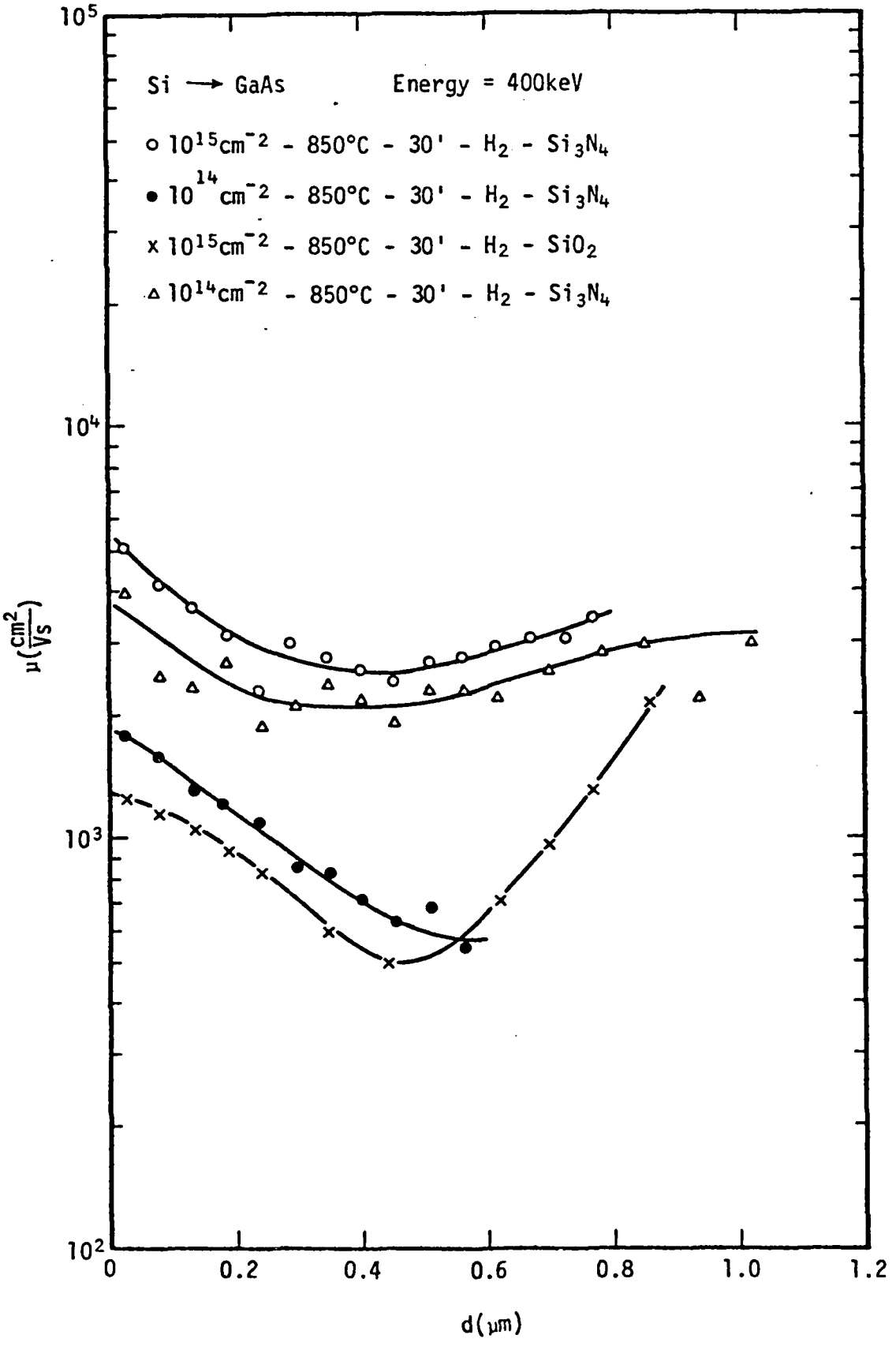

Fig. 4.1-3 Mobility profiles in Si-implanted GaAs

Table 4.1-1

Approximate Sheet Resistance (Ω/□) of Si Implanted GaAs Samples Annealed as Shown

Dose (ions/cm^2)	850°		900°	
	Si_3N_4	SiO_2	Si_3N_4	SiO_2
1 x 10^{13}	187	246	155	--
1 x 10^{14}	53	62	38	41
1 x 10^{15}	37	82	--	75

samples. The results using silicon nitride caps are strikingly different from those using silicon dioxide caps. In particular, the effect of increasing the dose from 10^{14} to 10^{15} ions/cm^2 seems quite different with the two different caps. This behavior is not understood at present.

It is clear from the present work that silicon implantation carried out at room temperature may be quite useful in the fabrication of GaAs IC's. In order to clarify the behavior of Si implants as a function of implanted dose, we intend to carry out further measurements at several difference doses concentrating primarily upon results obtained with a reactively sputtered silicon nitride cap.

4.2 Device and Circuit Fabrication (Science Center)

In this section, a brief discussion of several basic fabrication approaches is followed by a detailed description of the fabrication sequence being developed, and by our progress in fabrication. A short paragraph on plans concludes this section.

Different fabrication approaches have been taken for GaAs integrated circuits. One approach being pursued by other workers[7-9] is based on a mesa isolated fabrication scheme which follows closely the established fabrication of discrete microwave GaAs FETs. It enables the use of epitaxial material but results in a nonplanar structure which is less well suited to high-complexity, large-scale integration than to the small-scale integration, very high-speed, high-power circuits to which it is being applied. Substitution of a full wafer implanted layer for the epitaxial active layer could eliminate some of the problems of reproducibility and non-uniformity usually associated with epitaxial material. Replacement of proton damage isolation for mesa etched isolation could provide the desired planar structure. These improvements, however, allow the use of only a single active layer. An optimum process should be capable of at least two different active layer regions, one for diodes and one for FET channels. Additional high carrier concentration regions for ohmic contacts may also be desirable.

The above considerations have led us to the choice of a novel process based on multiple pocket implantation as the fabrication scheme best able to provide planar structures with optimized doping in each implanted pocket.

The fabrication sequence being developed can be characterized as a planar process with multiple pocket ion implantations through a dielectric layer. The circuit is fabricated through a silicon nitride layer which protects the semiconductor surface throughout processing and thereafter. Implantation is masked by photoresist only. The ions pass through the thin nitride layer into the semiconductor. Multiple implants are masked by different photo mask patterns to allow simultaneous optimization of diodes, FET channels and ohmic contacts. A single high-temperature anneal activates all of the implantations. (See Section 4.1). A two-layer annealing cap, consisting of silicon dioxide deposited on top of the remaining nitride, is used. This cap remains in place after anneal to protect the semiconductor surface. Windows are cut in this composite layer by plasma etching to allow formation of contacts and of Schottky diodes and gates. Definition of metals, ohmic and Schottky/first layer interconnect is done by lift-off. The lift-off process consists of formation of windows in photo resist followed by deposition of metal. The metal passes through the window adhering to the semiconductor below. Excess metal is lifted away when the photo resist is

removed by a solvent. The resulting structure consists of an approximately planar film completely covering the semiconductor surface. Second level interconnects are accomplished in a very similar manner after depositing a dielectric film to insulate between metal levels.

The fabrication sequence is illustrated in Fig. 4.2-1. Three typical devices are illustrated: an FET, a logic diode and a level shifting diode. The FET requires a moderately doped (n^-) channel and heavily implanted ohmic contacts (n^{++}). The logic diodes require a layer (here called n^+) also moderately doped, but deeper than the FET channel to avoid large series resistance. The level shifting diode requires a heavy implant like the ohmic contacts to minimize series resistance. In Fig. 4.2-1, the n^- implant is shown; in B and C, n^+ and n^{++} implants are shown. The n^{++} implant is considered optional at this point in the program. The mask set described in Section 4.4 includes test patterns and comparison devices which should allow us to evaluate the benefits of this implant. Figure 4.2-1(D) illustrates the composite annealing cap. E and F show contact metalization and Schottky/first layer interconnect metalization applied through windows cut in the dielectric layer. Note that the resulting structure is approximately planar. The fabrication process is completed as shown in G and H by deposition of a dielectric, cutting via windows and patterning of second level metalization.

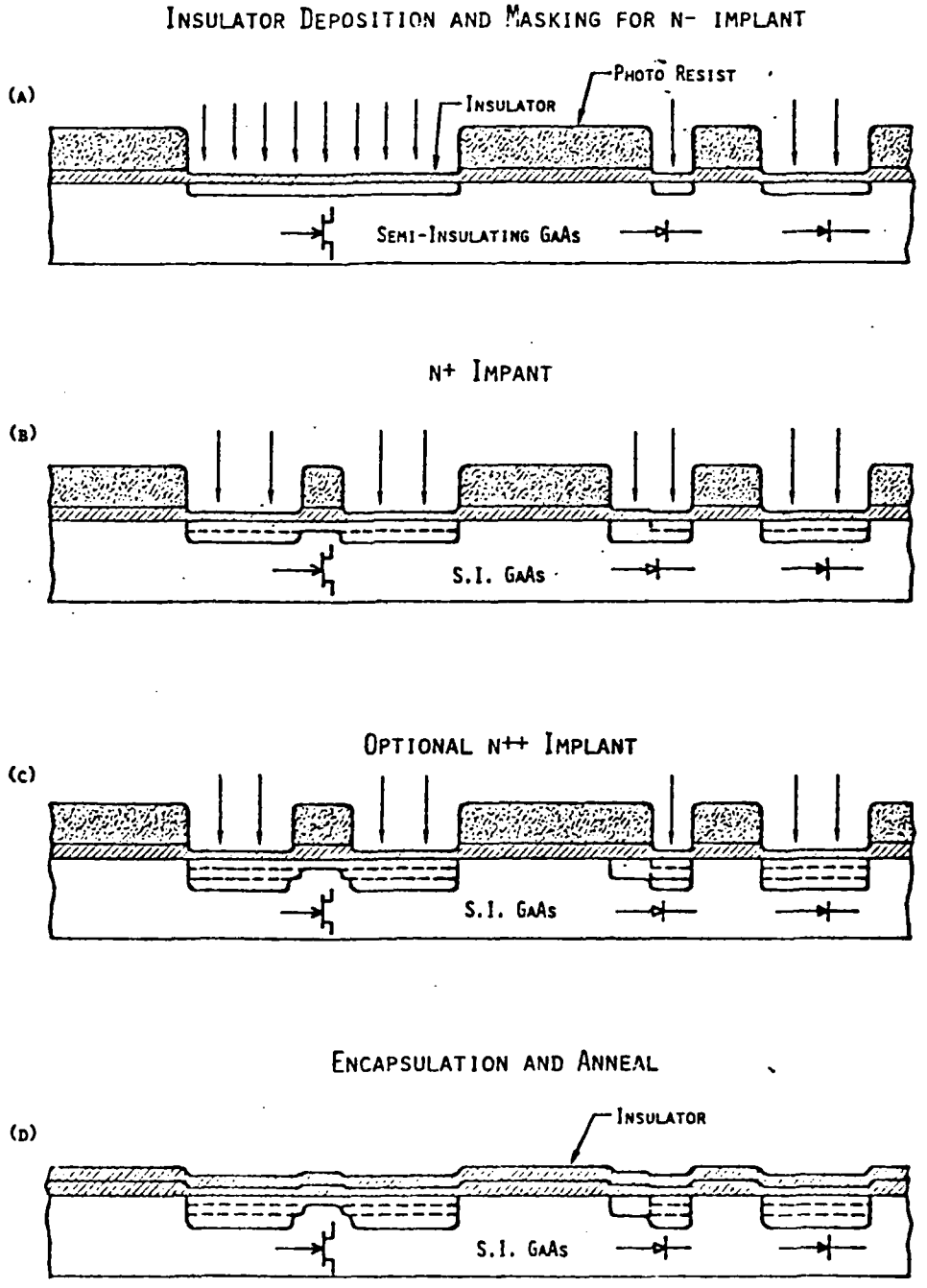

Fig. 4.2-1 Planar GaAs IC fabrication steps

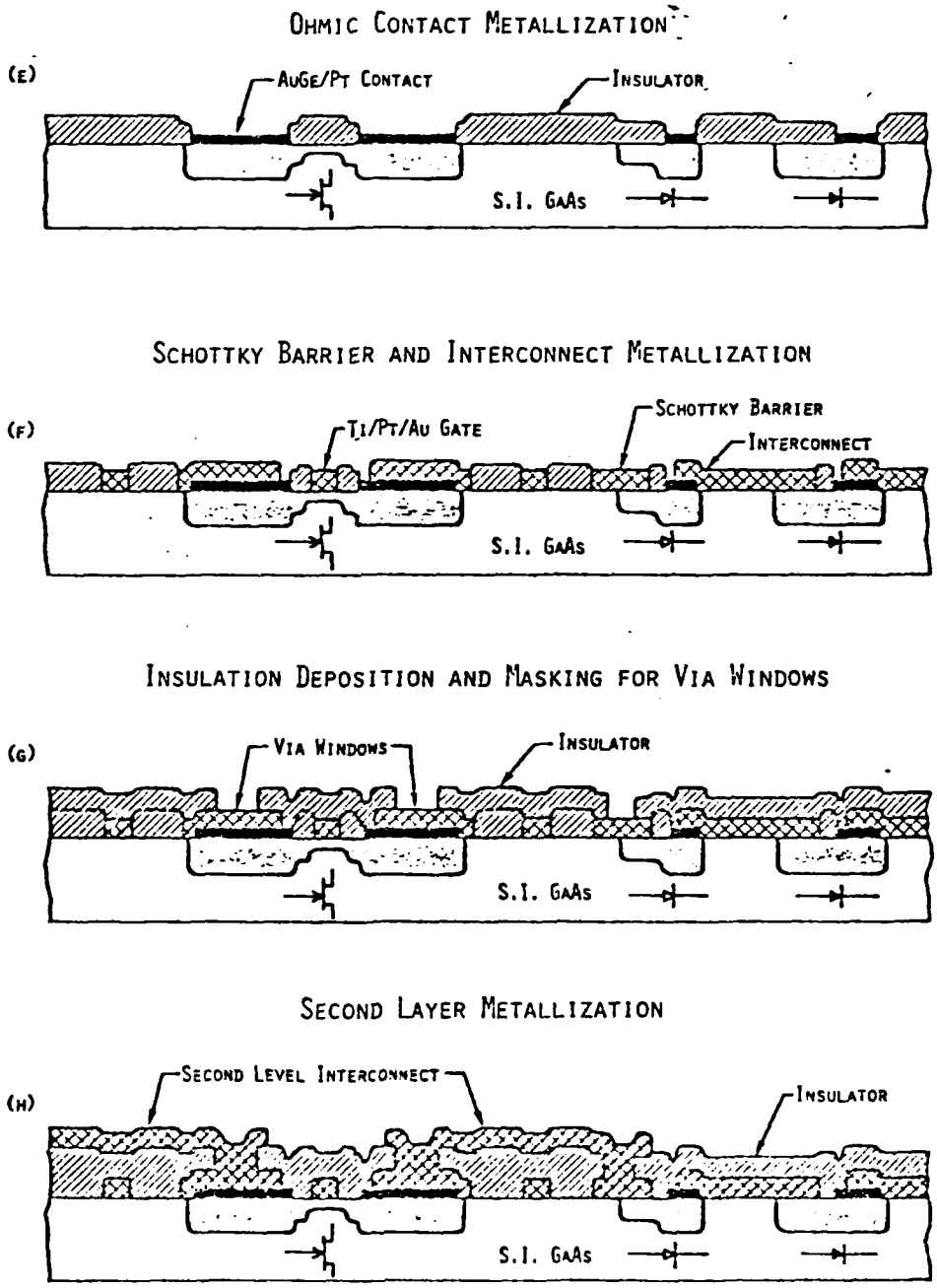

Fig. 4.2-1 Planar GaAs IC fabrication steps

The fabrication sequence described in this section should be regarded as under development, not finalized or optimized. It may be modified as necessary as the program progresses.

During the first three months of the program, significant progress was made in the area of device fabrication. While the first mask set of this program was being designed and fabricated, an existing mask set for 1-to-1 contact printing (developed under IR&D) was used to begin device fabrication. This mask set included both discrete FETs and diodes suitable for voltage-level shifting. The fabrication sequence described in the above (with a single implant) was carried out up through Schottky metalization, producing both FETs and diodes. This is a very important result because it demonstrates that the fabrication of isolated devices into implanted pockets embedded into the semi-insulating substrates, which is the key to our planar fabrication scheme, is a workable approach. Data from dc measurements made on devices, which were delivered in August 1977 under this contract, is summarized in Tables 4.2-1 and 4.2-2. The I_{dss} (drain-source current for zero gate-source voltage) for these devices was somewhat lower than expected for the channel implant dose and energy employed. The cause of this effect was traced to the cleaning procedure used just before gate deposition. The procedure removed more GaAs from the channel than had been anticipated, resulting in the lowered values of I_{dss}. This procedure, which was also likely the cause of the forward current saturation exhibited by the diodes, can be easily avoided in future runs.

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TABLE 4.2-1

DC Parameters for Planar FETs Fabricated by Ion Implantation in an IC Compatible Process

Device	I_{dss} @ 2.5V (ma)	V_{dss} (volts)	g_m @ V_g = 0 (mS)	V_{po} @ 10% I_{dss} (volts)	V_{po} @ 1% I_{dss}	Leads
1	1.9	1.3	2.4	0.95	1.2	yes
2	1.8	1.3	1.4	1.0	1.5	no
3	2.8	1.3	2.4	1.06	1.2	no
4	2.8	1.5	1.4	1.3	1.7	no
5	2.5	1.3	1.3	1.5	1.8	no

TABLE 4.2-2

DC Parameters for Planar Level Shifting Diode Pairs Fabricated by Ion Implantation in an IC Compatible Process

Device	V_f@ 4 a (volts)	R_f@ .1ma KΩ	V_b@ 10μa (volts)	I_r@ -10V (μa)	Center tap
1	1.0	15	40	< 1	yes
2	1.0	8.0	33	< 1	yes
3	1.0	8.0	35	< 1	yes
4	1.0	7.5	36	< 1	no
5	1.0	8.0	40	< 1	yes

During the next reporting period, the new mask set, described in Section 4.4, will be available. It will be used with the Canon 4-to-1 projection mask aligner to fabricate both test patterns and prototype integrated circuits by the planar multiple pocket implant scheme described above. Significant work is expected to be required to implement second-level metalization.

4.3 Contact Metalization Studies (Caltech)

During our previous ARPA supported work on GaAs technology, helium ion backscattering was applied to the study of the metallurgy of contact metalization systems for GaAs. We expect to continue this application of backscattering measurements on the present contract. It is desirable to be able to evaluate the electrical properties of contact metalization also. Metal masks have been prepared for the definition of contact patterns to be used in the measurement of specific contact resistance. We intend to study Au based contact metalization and other possible contact metal systems also. One such system being considered in the Pd-Si system, since the PdGe system is known to form good contacts on GaAs, and Si has a higher solubility in GaAs than that of Ge.

4.4 Mask Design

Mask design represents an important stage of this planar IC technology development program. A set of masks has been fully designed, the patterns have been digitized, and at the end of this reporting period the masks were being fabricated.[10] The main goal for this mask set was to implement and test the proposed fabrication process. Great attention was paid to the design of circuit components, namely FETs, active loads and diodes, and the way they were integrated into logic gates. A variety of design alternatives were incorporated into the masks in order to be able to determine optimum design rules. Simple circuits, linear chains and ring oscillators, were designed in order to test the performance of logic functions, and to obtain some preliminary results on power and speed.

Maximum process flexibility was allowed for in the design. For example, although the mask set was designed for a three implant process, the layouts are such that all the circuits can work with only two implants. Redundancy was another criterion, so that in every case when there was uncertainty between two designs, both were tested.

The mask set contains eight layers:

1. Alignment references. These are alignment marks to etch in the substrate as absolute references. This layer may be needed in case of deviations from the normal processing sequences.

2. N^- implant. This is the FET channel layer with a doping density of $10^{17}cm^{-3}$ and a thickness of 0.2 m (see Sec. 4.1).
3. N^+ implant. This is the implant for logic diodes. It has a doping density similar to that of the n^- layer, but it is deeper in order to lower the series resistance. This layer has also been extended under the ohmic contacts and level shifting diodes as a substitute for the n^{++} layer if it is not used.
4. N^{++} implant. This is a heavy dose implant for ohmic contacts and for level shifting diodes, which require very low series resistance (see Sec. 4.1).
5. Ohmic metalization. Used to form the ohmic contacts.
6. Schottky metalization. This layer includes the FET gates, the Schottky diodes and all the first layer interconnects.
7. Windows. This layer contains the vias in the dielectric that insulates the first and second layer metalization, to be opened for first to second layer interconnects.
8. Second layer metalization. This is used whenever required by overcrossings.

The mask layout is shown in Fig. 4.4-1. The top portion of this figure shows how the mask is organized into 9 chips, with a process monitor

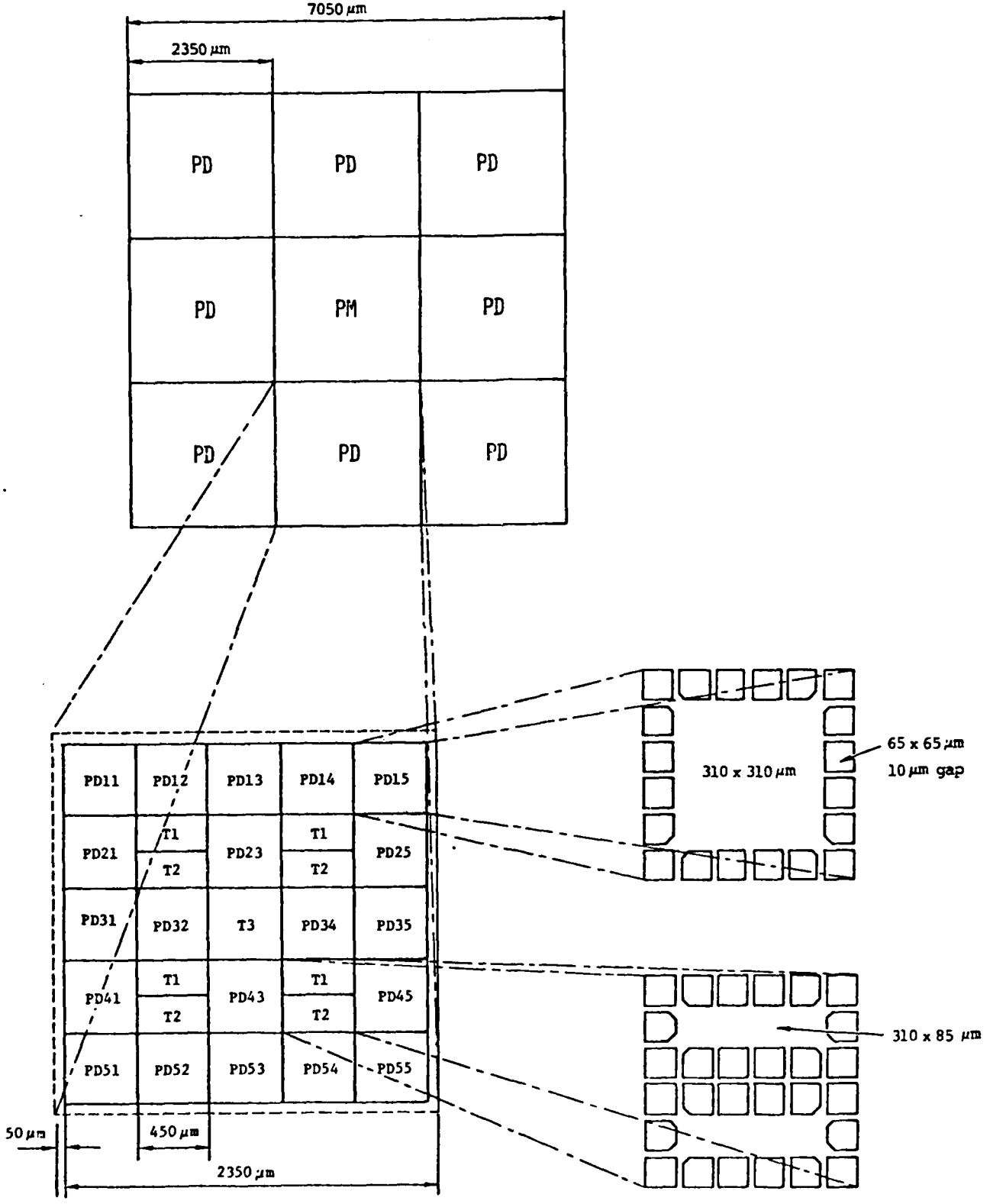

Fig. 4.4-1 Mask schematic

(PM) chip in the center, surrounded by 8 identical process development (PD) chips. The dimensions indicated in the figure are final dimensions on the wafer. The mask is actually four times larger because it will be used on a 4X projection mask aligner. The mask will be stepped by the projection mask aligner.

Each chip is subdivided into an array of 5x5 lots, as indicated at the bottom left corner of Fig. 4.4-1. The size of each lot is 450x450μm. The lots are labeled with matrix notation. There are five exceptions, lots 22, 24, 42 and 44 labeled T1/T2, and lot 33 labeled T3. T1, T2 and T3 are special test lots. They are common to the PM and PD chips, and they are more dense on the chip than regular lots in order to gather more statistical information, and in order to obtain better information on uniformity on the wafer. These lots will be the mostly used for automatic probing (see Sec. 5.1). At the bottom right of Fig. 4.4-1 the two contact configurations used are shown. The size of the contact pads is 65x65μm. The distance from center to center is 75μm, a distance quite compatible with the capability of probe card manufacturers.

Figure 4.4-2 is a schematic of the lot assignment in the PM chip. This chip makes use of some test patterns developed by the National Bureau of Standards.[11] Lots PM11, PM13, PM15, PM31, PM35 and PM51, labeled C-V, have large Schottky diodes ($10^{-3}cm^2$) made on each implant and on each

PM CHIP

	1	2	3	4	5
1	C-V n^-	SM Test Overcrossings	C-V n^+	Overcrossings	C-V n^{++}
2	Interconnects SM to 2M	T1 T2	Ohmic Contacts	T1 T2	2M Test n^-,n^+ Lines
3	C-V n^-+n^+	Van der Pauw n^-, n^+ n^-+n^+	T3	Van der Pauw n^{++} n^-+n^{++} $n^-+n^++n^{++}$	C-V n^-+n^{++}
4	Interconnects SM to $n^-+n^++n^{++}$	T1 T2	MO n^-	T1 T2	OM Lines n^{++} Lines Ellipsometry
5	C-V $n^-+n^++n^{++}$	Isolation n^+-n^+ n^+-n^+ corner n^+-SM OM-OM	MO $n^-+n^++n^{++}$	Isolation n^{++}-n^{++} n^{++} n^{++} corner n^{++}-SM SM-SM	MOM

SM ≡ Schottky Metallization
2M ≡ Second Layer Metallization
OM ≡ Ohmic Contact Metallization
n^- ≡ n-type implant for FET active layers
n^+ ≡ n-type implant for logic diodes
n^{++} ≡ n-type implant for ohmic contacts

Fig. 4.4-2 Lot assignment for the process monitor (PM) chip

practical combination of implants. Instead of having one ohmic contact, these diodes have two contacts, one of each side of the capacitor, so that they have the configuration of fat FETs. Such fat FETs can be used to profile the electron mobility in addition to the carrier concentration.[12] Lots PM32 and PM34 have Van der Pauw patterns[11] for sheet resistance measurements on different combinations of implants. Lots PM43, PM53 and PM55 contain capacitors formed between the second layer metal and either an implanted layer or a first layer metal for evaluation of the dielectric layer which isolates the first and second layer interconnects.

Lots PM52 and PM54 (Fig. 4.4-2) are designed to test how well the substrate retains its insulating properties after processing. The test patterns consists of pairs of pockets implanted into the semi-insulating substrate with gaps of 1, 2, 3, 5, and 8μm. Ohmic contacts are made on the implanted pockets. The pockets are either n^+ or n^{++}. There are also isolation tests between implanted layers and Schottky metal, between Schottky metal layers and between ohmic metal layers.

Lots PM12, PM25 and PM45 (Fig. 4.4-2) contain lines of Schottky metal, second layer metal and implants designed to test the lithography and to study interconnect resistance. Meander lines are also tested in view of the fact that corners tend to be critical in the photoresist process.

Lots PM12 and PM14 allow to evaluate overcrossings between first and second layer metalization by testing for open lines and for shorts between the lines.

Lot PM23 (Fig. 4.4-2) contains ohmic contact tests. The contact resistance will be determined using a variable gap configuration to subtract the n^- channel resistance. [13] The resistance of contacts made directly on the n^- channel will be compared with that of contacts with an additional n^+ or n^{++} implant in order to determine how effective the added implant is in lowering the contact resistance.

The special lot T1 for more frequent tests is a distillation product of the PM chip. It contains the most critical sheet resistance measurement (on n^-), and the most important ohmic contact and isolation tests (using both n^+ and n^{++} implants).

The process development (PD) chip will now be described. This chip contains isolated components, gates and full circuits. A schematic of lot assignments is shown in Fig. 4.4-3. Five lots are assigned to FET design. Lots PD23, PD32 and PD43 compare a set of 1 and 2μm gate FETs of different width. The same devices are placed in all three lots, but they have n^+ and n^{++} implanted contacts in one lot, only n^+ implanted contacts in the second lot, and no additional implant in the contacts in the third lot. This

PD CHIP

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	1	2	3	4	5
1	20 μm LC+RO No 2M LS	Active Loads $n^-, n^+ + n^{++}$ L_g = 1,2 μm	FETs Multiple Gates	10 μm LC+RO No 2M No LS	20 μm LC+RO No 2M No LS
2	Diodes Logic n^+ Level Shifters AM	T1 T2	FETs n^-	T1 T2	Diodes Logic n^- Logic n^{++} AM Res. Pat.
3	Gate Design	FETs n^-, n^+	T3 10 μm LC+RO No 2M LS	Gates	Backgating Active Loads $n^-, n^+ + n^{++}$
4	3 μm, 5 μm LC+RO No LS AM	T1 T2	FETs n^-, n^+, n^{++}	T1 T2	3 μm, 5 μm LC+RO LS AM
5	20 μm LC+RO 2M LS	10 μm LC+RO 2M LS	FET Design n^-, n^+, n^{++}	10 μm LC+RO 2M No LS	20 μm LC+RO 2M No LS

LC ≡ Linear Chain
RO ≡ Ring Oscillator
LS ≡ Level Shifting Diode
2M ≡ Second Layer Metallization
AM ≡ Alignment Marks

Fig. 4.4-3 Lot assignment for the process development (PD) chip

test, in conjunction with the contact resistance measurements is designed to evaluate the advantages of multiple implants. Lot PD13 contains different designs of multiple gate FETs. Lot PD55 investigates design alternatives for the overlapping of the different layers at the edges of FET sources and drains. Lots PD21 and PD25 contain tests of diodes. The diodes are arranged either in groups of 10 in series (with taps) or 200 in parallel.

Lot PD12 (Fig. 4.4-2) contains a study of active loads of several width and gate lengths. Two basic designs are compared, one like a regular FET with its gate connected to the source, the other having the gate made of a layer of Schottky metal extending from the source into the channel.

Lots PD31 and PD35 address the question of backgating of one device by the substrate polarized by a neighboring device operating at a different voltage. In lot PD35, a large contact is implanted into the substrate near an active load in order to study the effect of its potential on the I-V characteristic of the active load. Guarding tests are conducted by extending a strip of implanted material or Schottky metal from the active load drain between the active load and the neighboring contact. This type of guarding or shielding is also the basis for different alternatives in gate design explored in lot PD31.

The special lot T2 (Figs. 4.4-2 and 4.4-3) is a distillation product of the lots of the PD chip described above. It contains a 1μm gate FET and a

1μm active load, and a full two input Schottky diode NOR gate, with dimensions representative of those employed in the circuits. Each electrical point of the gate is connected to a pad, so that T2 can be used either to test individual components or to test the full gate function at low frequency.

The remaining eight lots on the PD chip (Fig. 4.4-3) contain circuits. Each lot has a linear chain and a 7 or 9-stage ring oscillator. In each case, not being clear whether a level shifter diode in series with the logic diodes will be required, the same circuits have been designed with or without such level shifter, as indicated in Fig. 4.4-3. In this figure, the circuits are labeled according to the width of the FET in the logic gate as 20, 10, 5 and 3μm linear chains and ring oscillators. In each case, the active loads are scaled to the FET dimension so that they properly limit the current while providing sufficient fanout. As indicated in Fig. 4.4-3, circuits have been designed so that they either require or do not require a second layer metalization. In the circuits without second layer metalization the power lines cross under the signal lines by means of heavy dose implants. Polarities were taken into account so that the Schottky metal was always reverse biased with respect to the implant line at each overcross. The approach without second layer metalization is not being considered as a final substitute for the second layer metalization because it does not allow

for sufficient design flexibility, and the series resistance of the implant undercrossings may be an undesirable feature. However, it has been pursued as a means to fabricate working circuits without waiting for the second layer metalization process to be developed.

In summary, a complete mask set for process development has been designed. This mask set contains tests for monitoring and evaluating different stages of the fabrication process, it contains a variety of design alternatives for the circuit components so that optimum design rules can be investigated, and it integrates the components into logic gates and simple circuits like linear chains and ring oscillators for some test of logic functions and some preliminary speed measurements.

5.0 DEVICE MODELING AND TESTING

This section will cover two subjects, the construction of an automatic measurement system, and the analytical study of switching speed limits. Both areas are still at their preliminary stage, since larger emphasis was placed on materials and on process development at this early stage of the program.

5.1 Automatic Test System (Science Center)

In order to be able to probe a large number of wafers and gather sufficient statistical information, an automatic measurement system is necessary. Such a system has been designed and is being constructed, partly with company funds. This system will be used for dc measurements. A separate measurement system will be used for high speed characterization.

The automatic dc measurement system being built is based on Electroglas, Model 1034X, Automatic Prober. The prober and the measurement system are controlled by a Data General Eclipse minicomputer operating under AOS (Advanced Operating System) which gives it multiuser capability. The computer has 120K words of CP memory. It is equipped with four discs, a magnetic tape unit and a line printer. This computer system is being used for general data acquisition at department level, and its hardware will be

further expanded as needed. The prober operator will interface with the computer via a dedicated Tektronix 4010 display with graphics capability.

A block diagram of the measurement system is shown in Fig. 5.1-1. Except for manual alignment of the wafer, the computer has full control of the prober. Each of 20 probes (from a probe card or micromanipulators) can be automatically connected to any of 10 measurement channels. Among such measurement channels are five digital to analog converters (DACs) which output to the probes the voltage set by the computer and return to the computer the value of the current measured by a current amplifier. Two DACs, called HC DACs in Fig. 5.1-1, are designed for larger currents so that they can be used as supplies, while the other three DACs labeled LC DACs are designed for lower currents, to be used as signal sources. The other measurement channels are a current supply, a ground, and two inputs connected to a floating A/D converter for floating voltage measurements. One additional measurement channel was left unused for further applications. All the measurement units are interfaced with the computer through a Hewlett Packard, Model 6940 multiprogrammer, which takes care of the communication protocol between the computer and 15 digital or analog input or output interface cards. An extender has been added so that the capacity has been increased to 30 card slots.

C-V measurements are handled by separate probes bypassing the cross point switch which would add too much parasitic capacitance. Except for this

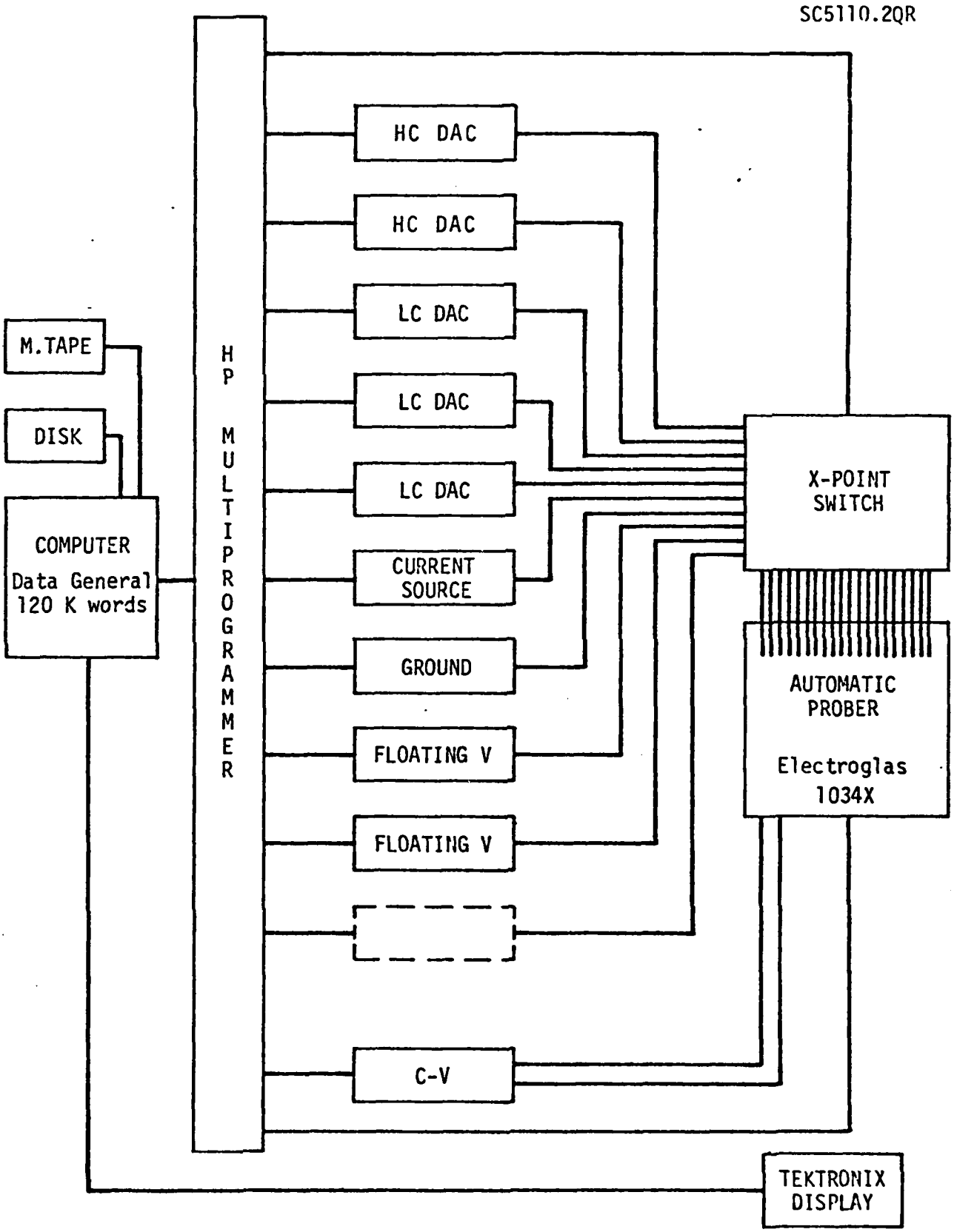

Fig. 5.1-1 Block diagram of the automatic dc test system

bypass, the C-V measurements will be automatic. They will be done with a PAR 5204 lock-in amplifier, which will also be interfaced with the computer through the Hewlett Packard multiprogrammer.

At the end of this reporting period, the system had been completely designed and partly built. The computer system was fully operational, as well as the hardware and software for the computer-multiprogrammer interface. Construction and testing of the rest of the system is in progress.

A separate system will be set up for high-speed measurements. This system will use a custom built prober which is currently being built. This prober will be automatically controlled by an Apple II microcomputer.

5.2 Switching Speed Analysis (Cornell University)

The objective of this task is to analyze the physical limits on power-delay product, propagation delay and power per logic gate for GaAs MESFET logic, to relate these parameters to material and design characteristics of the devices, and to develop a two-dimensional computer model of a FET which can be used for computer-aided analysis of GaAs integrated circuits.

The first step was the development of a two-dimensional computer model for GaAs FETs. Several computer simulations of GaAs FETs have been performed, but they require long computation times. For this reason their

usefulness for computer-aided analysis is limited. Our idea was to develop a semi-analytical model which takes into account all important physical factors but require much smaller computation times. In our approach the device is divided into three areas: source-gate and gate-drain regions where the electric field is relatively small, the region under the gate, and the high-field stationary Gunn domain which is formed near the drain side of the gate. The field under the gate is two-dimensional, the field distribution being given by the analytical solution of the Poisson equation with one unknown parameter. This parameter is defined via an iteration process so that current continuity is satisfied. The computer program for this calculation has been developed and debugged.

The computation time is only approximately 1/4 sec per point (compared to a minute or more for a conventional two-dimensional computer calculation). Some of the results obtained are depicted in Fig. 5.2-1 where the computed current-voltage characteristics of a GaAs FET are shown. Note the region with static negative differential resistance related to the Gunn domain formation. The upper curve illustrates the influence of large leakage through the substrate (a low substrate source-drain resistance R_S = 5000 ohms was assumed).

The above model will be used as a tool to study the switching parameters for GaAs FETs. With this model, it is possible to calculate the

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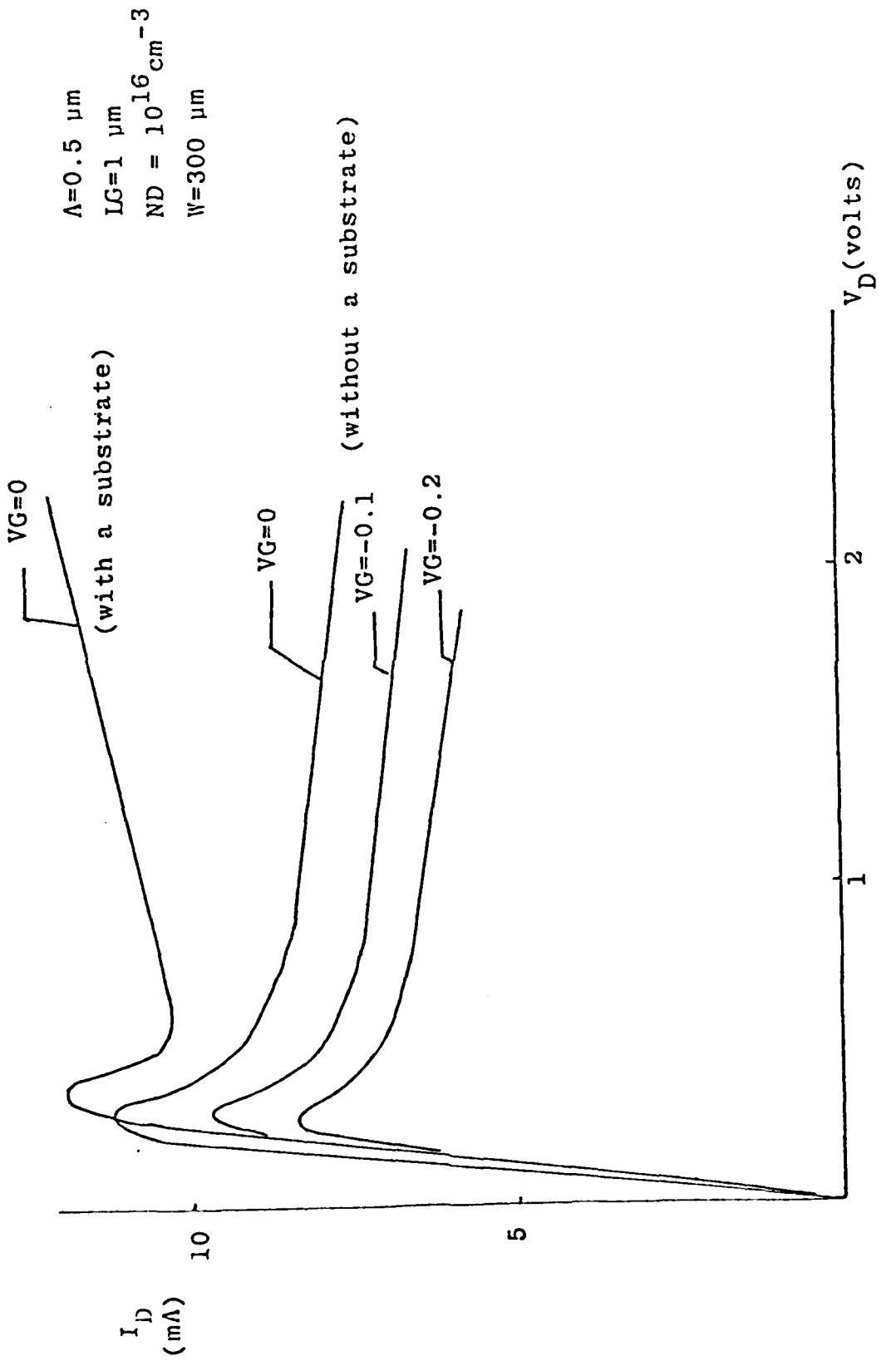

Fig. 5.2-1 Computed current voltage characteristics of FETs

amount of charge under the gate and to investigate the dependence of switching parameters on material and design parameters. It is also possible to calculate small-signal parameters of FETs and to use them to optimize the design parameters of GaAs FET amplifiers. The field distributions under the gate predicted by the model will be used to investigate the overshoot effects under the gate[14,15] in order to establish the ultimate limit for switching time which is determined by electron energy relaxation time.

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